REMARKS

The present application was filed on October 30, 2003 with claims 1-15. Claims 1, 7-9 and 15 are the independent claims.

In the outstanding Office Action, the Examiner: (i) objected to the figures; (ii) rejected claims 1-6 and 9-14 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,122,336 to Anderson (hereinafter "Anderson"); (iii) rejected claim 15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,133,773 to Garlepp et al. (hereinafter "Garlepp"); and (iv) rejected claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over Anderson in view of U.S. Patent No. 6,295,328 to Kim et al. (hereinafter "Kim").

In this response, Applicants: (i) amend FIGs. 1A, 1B, 2A and 2B; and (ii) traverse the various §102(b) and §103(a) rejections for at least the following reasons.

Regarding the figures, Applicants have added a prior art legend to FIGs. 1A, 1B, 2A and 2B as requested by the Examiner. Withdrawal of the objection is respectfully requested.

With regard to the issue of whether claims 1-6 and 9-14 are anticipated under 35 U.S.C. §102(b) by Anderson, the Office Action contends that Anderson discloses all of the claim limitations recited in the subject claims. Applicants respectfully assert that Anderson fails to teach or suggest all of the limitations in claims 1-6 and 9-14, for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Applicants assert that the rejection based on Anderson does not meet this basic legal requirement, as will be explained below.

The present invention, for example, as recited in independent claim 1, recites a voltage-controlled delay line, comprising a delay element, and a phase interpolation circuit coupled to the delay element, wherein the delay element and the phase interpolation circuit are operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal. Independent claim 9 recites similar limitations.

Furthermore, as illustratively explained in the present specification at page 1, lines 15-23:

> Principles of the present invention provide a phase interpolation technique for voltage-controlled delay line (VCDL) implementation. The techniques of the invention may employ a second-order phase interpolation topology to improve tuning range performance of the VCDL over process and temperature variation. In one aspect of the invention, the technique may use a complementary input signal to set an absolute 180-degree phase reference. As a result, the maximum (complete or full) tuning range of 180 degrees can be achieved regardless of internal delay variation. Such techniques may be employed in various circuits and systems, e.g., a delay-locked loop (DLL) circuit or a clock-and-data recovery (CDR) system. (Underlining added for emphasis)

Thus, as recited in independent claims 1 and 9, the delay element and the phase interpolation circuit are operative to use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

Anderson, as disclosed at column 3, lines 1-5, increases resolution of its frequency synthesizer by using interpolation to increase the number of clock phases. FIG. 4 of Anderson shows a ring oscillator and phase interpolation unit. However, despite the assertion in the Office Action, Anderson does not disclose a delay element and a phase interpolation circuit operative to use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claims 1 and 9.

First, Anderson does not disclose use of the input signal and the complement of the input signal to perform a phase interpolation process. The Examiner points to signals A0 and A1 in FIG. 4 of Anderson, however, these are not the input signal and the complement of the input signal. As explained at column 4, lines 2-4, these signals are merely clock phases generated by the ring oscillator and sent to the phase interpolation unit. Second, Anderson merely increases resolution of the frequency synthesizer by adding more clock phases. Anderson clearly does not provide a complete delay tuning range with respect to the input signal, as recited in independent claims 1 and 9.

For at least these reasons, Applicants assert that independent claims 1 and 9, and the claims that depend therefrom, are patentable over Anderson.

Regarding claim 15, the Office Action asserts that Garlepp discloses all the limitations in said claim. Applicants strongly disagree. While Garlepp, at column 4, lines 36-43, discloses a phase interpolator circuit which provides tunability of phase interpolation performance, Garlepp clearly does not disclose using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claim 15.

The phase interpolator tunability disclosed by Garlepp is realized via controllable capacitive loading, as clearly stated at column 4, line 37 and 38, of Garlepp. That is, Garlepp does not use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, as recited in independent claim 15. In fact, while Garlepp mentions an extended range for its adjustable phase interpolator (column 3, lines 31-34), Garlepp makes no mention of a realization of a complete delay tuning range with respect to the input signal, as in the claimed invention.

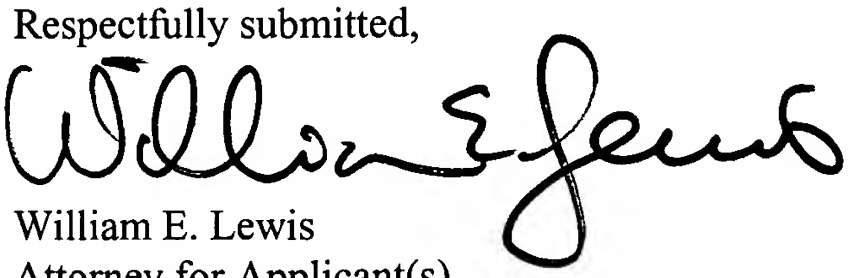
For at least these reasons, Applicants assert that independent claim 15 is patentable over Garlepp.

Regarding the §103(a) rejection of claims 7 and 8 based on the combination of Anderson and Kim, Applicants assert that such claims are patentable over the combination due at least to the above-mentioned deficiencies in Anderson. That is, claim 7 recites using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal, and claim 8 recites using the clock signal and the complement of the clock signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the clock signal. Based on the remarks above with respect to Anderson in terms of claims 1 and 9, it is clear that Anderson fails to disclose these limitations. Thus, the Anderson/Kim combination is deficient.

For at least these reasons, Applicants assert that independent claims 7 and 8 are patentable over the Anderson/Kim combination.

In view of the above, Applicants believe that claims 1-15 are in condition for allowance, and respectfully request withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,



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